REMARKS

Claims 1, 2, 5, 7, 11, 13, 14, 17, 19, 23, 25, 31, 35, 55, 60, 61, 72 and 74 are pending in the application. Applicants have amended claim 72. Support for the amendments is found, for example, from page 22 to page 25 and Figs. 4-7 of the specification. Accordingly, entry of this Amendment is respectfully requested.

Initially, Applicants would like to thank the Examiner for the indication that claims 13, 14, 17, 19, 23, 25, 31, 35 and 74 are allowable. The Examiner has objected to claims 11 and 68 as being dependent upon a rejected base claim, but indicated that the claims would be allowable if rewritten in independent form including all of the limitations of any intervening claims.

The Examiner has rejected claims 1, 55 and 72 under 35 U.S.C. § 102(e) as allegedly anticipated by U.S. Patent No. 6,383,916 issued to Lin ("Lin"). Applicants respectfully submit the rejection is overcome in view of the amendments and remarks herein.

To maintain a claim rejection under 35 U.S.C. § 102, a prior art reference must disclose each and every element of the claim. Lin fails to do so.

Claim 1 recites a semiconductor unit having two device terminals for every one input/output signal. The semiconductor unit comprises, *inter alia*, a laminated substrate having a main surface and a semiconductor chip having an input/output pad. The laminated substrate comprises at least two wiring layers, which include a signal wiring layer and a power-supply or ground-wiring layer. The semiconductor chip is mounted on the main surface of the laminated substrate through the input/output pad. The two device terminals are mounted on the laminated substrate. Significantly, the two device terminals are connected to the respective ends of a signal wire formed in the signal wiring layer and the signal wire is simultaneously connected to the

input/output pad through a via hole. In other words, both of the device terminals, and the input/output pad are electrically connected through a signal wire.

Claim 55 recites a semiconductor unit having at least two device terminals for every one input/output signal. The two device terminals are disposed in different sides of the semiconductor unit. Significantly, the two device terminals are wired to an input/output pad of a semiconductor chip that corresponds to the input/output signal. Thus, both of the device terminals, and the input/output pad are electrically connected through a signal wire.

Claim 72, as amended, recites a semiconductor unit comprising a semiconductor chip having an input/output pad and a package having a main surface and a back surface. The package comprises at least two ball terminal adhesive areas for every single input/output signal on the main and back surfaces of the package. Significantly, the two ball terminal adhesive areas are connected to each other through one of a via hole and a wire, and the via hole or wire is simultaneously connected to the input/output pad the semiconductor chip through a wire. Thus, both of the terminal adhesive areas and the input/output pad are electrically connected through a via hole/a wire and a wier.

Therefore, claims 1, 55 and 72 all recite the feature of a three way electrical connection among both of the terminal devices or the terminal adhesive areas, and the input/output pad of the semiconductor chip. The three way electrical connection can be implemented by a via hole, a wire or any proper combination thereof.

Lin discloses an integrated circuit structure, which allows arbitrary rerouting of input/output leads. Specifically, Lin discloses, in Fig. 10 thereof, a ball grid array (BGA) device 100 comprising contact balls 101 – 105, and a BGA substrate 130 comprising contact points 121-125 and wiring 131 provided within the substrate. By using the BGA substrate 130 and the

wiring 131, the BGA pads can be arranged in a different and arbitrary sequence that is required for further circuit design or packaging. For instance, the contact ball 101, which is on the far left side of the BGA device 100, could be rerouted to the location of the contact point 122 which is on the second far right of the BGA substrate 130. However, it is obvious from Fig. 10 and the disclosure of Lin that the wiring 131 only connects the corresponding contact balls and contact points, for example, the contact ball 101 and the contact point 122. The wiring 131 is not connected to another semiconductor element, for example, an input/output pad of a semiconductor chip.

Lin also discloses alternative wiring schemes in Figs. 9 and 11 thereof. However, none of the figures illustrate a three way wiring connection of two terminal devices and an input/output pad of a semiconductor chip.

Lin further discloses, in Fig. 5 thereof, an arrangement of power/ground pads combined with a signal pad. However, the pads arrangement of Fig. 5 is not relevant to a wiring connection of two terminal devices and an input/output pad of a semiconductor chip.

Lin further discloses, in Figs. 6 and 7 thereof, other semiconductor structures having contact points and pads connected by via holes. As illustrated in the figures, separate contact points 6 are connected respectively to pads 10, 23 and 26 through via holes 7 and 7'. Likewise, the structures of Figs.6 and 7 fail to disclose a three way connection among two terminal devices or two terminal adhesive areas, and an input/output pad of a semiconductor chip.

Therefore, Lin fails to disclose the features that two terminal devices or two terminal adhesive areas are connected by a wire or a via, and the two terminal devices or two terminal adhesive areas are further connected to an input/output pad of a semiconductor chip, as recited by claim 1, 55 and 72.

Since Lin fails to disclose each and every element of claims 1, 55 and 72, the rejection of the claims under 35 U.S.C. §102(e) based on Lin is overcome and withdrawal thereof is respectfully requested.

The Examiner has rejected claims 2 and 61 under 35 U.S.C. § 103(a) as being unpatentable over Lin in view of U.S. Patent No. 6,137,164 issued to Yew et al. ("Yew"). Applicants respectfully submit that the rejection is overcome in view of the remarks herein.

Claim 61 recites a semiconductor unit having two device terminals for every one input/output signal. The semiconductor unit comprises a laminated substrate and two semiconductor chips each having an input/output pad. Likewise, claim 61 recites a three way electrical connection among both of the device terminals, and the input/output pads of both semiconductor chips. Specifically, the two device terminals are connected to each other through a via hole, and the via hole is simultaneously connected to the input/output pads of the two semiconductor chip through a wire.

Claim 1, from which claim 2 depend, is discussed above. Lin is discussed above.

As discussed above, Lin fails to disclose or suggest a three way electrical connection among two device terminals and the input/output pad of the semiconductor chip through a via hole and/or a wire.

Yew discloses an assembly for stacking IC devices. However, Yew fails to disclose the above features, thus cannot overcome the underlying deficiencies identified in Lin. Therefore, Lin and Yew, taken alone or in any proper combination, fail to disclose or suggest the combination of features, as recited in Claims 2 and 61. Accordingly, the rejection of claims 2 and 61 under 35 U.S.C. § 103(a) over Lin in view of Yew is overcome and withdrawal thereof is respectfully requested.

The Examiner has rejected claim 5 under 35 U.S.C. § 103(a) as unpatentable over Yew in view of U.S. Patent No. 6,630,628 issued to Devnan et al. ("Devnan"). Applicants respectfully submit that the rejection is overcome in view of the remarks herein.

Claim 1, from which claim 5 depend, is discussed above. Yew is discussed above.

As shown above, Yew fails to disclose or suggest a three way electrical connection among two device terminals and the input/output pad of the semiconductor chip through a wire and/or a via hole.

Devnan discloses a high-performance laminate for integrated circuit interconnection. Likewise, Devnan fails to disclose the above features, thus cannot overcome the underlying deficiencies identified in Yew. Therefore, Yew and Devnan, taken alone or in any proper combination, fail to disclose or suggest the combination of features, as recited in claim 1, from which claim 5 depends. Accordingly, the rejection of claim 5 under 35 U.S.C. § 103(a) over Yew in view of Devnan is overcome and withdrawal thereof is respectfully requested

The Examiner has rejected claims 7 and 60 under 35 U.S.C. § 103(a) as unpatentable over Lin in view of U.S. Patent No. 6,184,477 issued to Tanahashi ("Tanahashi"). Applicants respectfully submit that the rejection is overcome in view of the remarks herein.

Claim 60 recites a semiconductor unit having two device terminals for every one input/output signal. Likewise, claim 60 recites a three way electrical connection among both of the device terminals, and the input/output pad of a semiconductor chip. Specifically, the two device terminals are connected to each other through a via hole, and further connected to the input/output pad of the semiconductor chip through a wire.

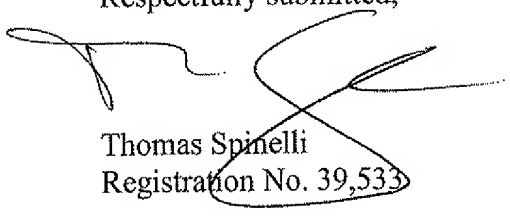
Claim 1, from which claim 7 depend, is discussed above. Lin is discussed above.

As shown above, Lin fails to disclose or suggest a three way electrical connection among two device terminals and the input/output pad of the semiconductor chip through a wire and/or a via hole.

Tanahashi discloses a multi-layer circuit substrate having orthogonal grid ground and power planes. Likewise, Tanahashi fails to disclose the above features, thus cannot overcome the underlying deficiencies identified in Lin. Therefore, Lin and Tanahashi, taken alone or in any proper combination, fail to disclose or suggest the combination of features of claims 7 and 60. Accordingly, the rejection of claims 7 and 60 under 35 U.S.C. § 103(a) over Lin in view of Tanahashi is overcome and withdrawal thereof is respectfully requested.

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims presently pending in the application are believed to be in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



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